M.S. THESIS

Study on Random Telegraph Noise in Nano-wire and Saddle Device Using Simulation

나노와이어와 Saddle 구조에서 시뮬레이션을 이용한 RTN 분석

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ABSTRACT

A 70-Å nano-wire field-effect transistor (FET) for sub-10-nm CMOS technology is designed and simulated in order to investigate the impact of an oxide trap on random telegraph noise (RTN) in the device. It is observed that the drain current fluctuation ($\Delta I_D/I_D$) increases up to a maximum of 78 % due to the single electron trapping. In addition, the effect of various trap positions on the RTN in the nano-wire FET is thoroughly analyzed at various drain and gate voltages. As the drain voltage increases, the peak point for the $\Delta I_D/I_D$ shifts toward the source side. The distortion in the electron carrier density and the conduction band energy when the trap is filled with an electron at various positions in the device supports these results.

Random telegraph noise (RTN) magnitude in the Gate Induced Drain Leakage (GIDL) current of Saddle MOSFET, a promising candidate for high-density DRAM applications, is analyzed using three-dimensional simulation TCAD. We simulated the RTN

magnitude in GIDL with various trap positions. The distortion in the electron field distribution when the trap is filled with an electron at various positions in the device supports these results.

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Keywords : Nano-wire, Saddle, Random Telegraph Noise (RTN), 3-D Simulation, Trap.

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CONTENTS

1. Introduction

As the feature size of the modern field-effect transistors (FETs) is scaled down below 10 nm, the short channel effect in the electron devices is one of the most difficult technical challenges. As the critical dimensions shrink to a few nanometers, non-conventional device structures that can successfully suppress the short channel effect have been proposed. For example, double-gate FinFET [1-2], Fully-Depleted Silicon-on-Insulator (FD-SOI) MOSFET [3-4], and gate-all-around (GAA) MOSFET [5-10] have attracted much attention in the industry. Among them, the nano-wire FET has the highest gate-to-channel capacitive coupling primarily because the channel is surrounded and controlled by the gate in all directions, and therefore, silicon nano-wire architecture is the most attractive structure for sub-10-nm CMOS technology. Because even the extremely scaled sub-10-nm device has several defects, random telegraph noise (RTN) created by an

oxide trap plays an important role in analyzing device performance [11-13]. The sub-10-nm nano-wire FET should be designed considering the impact of oxide traps on its performance. However, there is currently no study on the impact of RTN created by a single-trap in a 70-Å nano-wire FET, to the best of authors' knowledge. In this work, the critical effect of a single trap on the performance variation of a 70-Å nano-wire FET is discussed in detail, and the impact of various oxide trap positions on the drain current fluctuation is quantitatively analyzed.

Moreover, Recently the recess-channel-array transistor (RCAT) [14] and the RCAT-asymmetric channel doping (ASC) [15] based on recess channel structure have been proposed to reduce possible cell leakage current. One of the promising structures to solve these problems is the saddle MOSFET [16-17], which has the electrode wrapping the recessed surface and side surface. The saddle MOSFET has advantages such as excellent short channel effect (SCE) immunity, high Ion, low drain-induced barrier lowering (DIBL), excellent sub-threshold swing (SS). In

this study, we studied 20 nm technology node Saddle MOSFET device using 3-D simulation tool.

Random telegraph noise (RTN) in GIDL current has been a serious concern in scaled down DRAM technology. The origin of RTN is attributed to trapping/de-trapping of carriers in trap, located in a gate oxide or at a Si/SiO_2 interface [18-19]. There are many researches which investigate the gate leakage current and GIDL current characterization, influenced by an oxide trap. The GIDL is an important leakage current in modern MOSFETs. That is mainly associated with both band to band tunneling and trap-assisted tunneling in a gate to drain overlapped region [20-21]. As a result, RTN in GIDL current is believed to cause variable retention time in DRAM devices. As device dimensions are minimized, RTN in GIDL current becomes dominant, therefore there has been much interest regarding RTN in GIDL current. In this paper, we propose an approach for RTN in GIDL current with Saddle MOSFET structure, a promising candidate for high-density DRAM applications, to determine its performance and reliability.

2. Nano-wire device simulation

2.1 Nano-wire device design

Based on the International Technology Roadmap for Semiconductors (ITRS), the nanowire FET design (Figs. 2. 1a and 2. 1b) for low-power sub-10-nm technology is optimized using three-dimensional (3-D) device simulations by selecting a channel length of 70 Å, a radius of 20 Å, a source/drain doping concentration of 10^{20} cm^{-3} to achieve a maximum drive current for an effective oxide thickness (EOT) of 10 Å, a gate work-function of 4.62 eV, and an off-state leakage current specification of ~ 10 pA/μm at 0.7-V power supply voltage. The input characteristic curves (*i.e.*, drain current *vs.* gate voltage) for three different drain voltages are shown in Fig. 1c with sub-threshold slope (SS) of 70 mV/dec and an on-state saturation drive current of ~145 μA/μm.

To investigate the effect of the trap position on RTN in the nano-

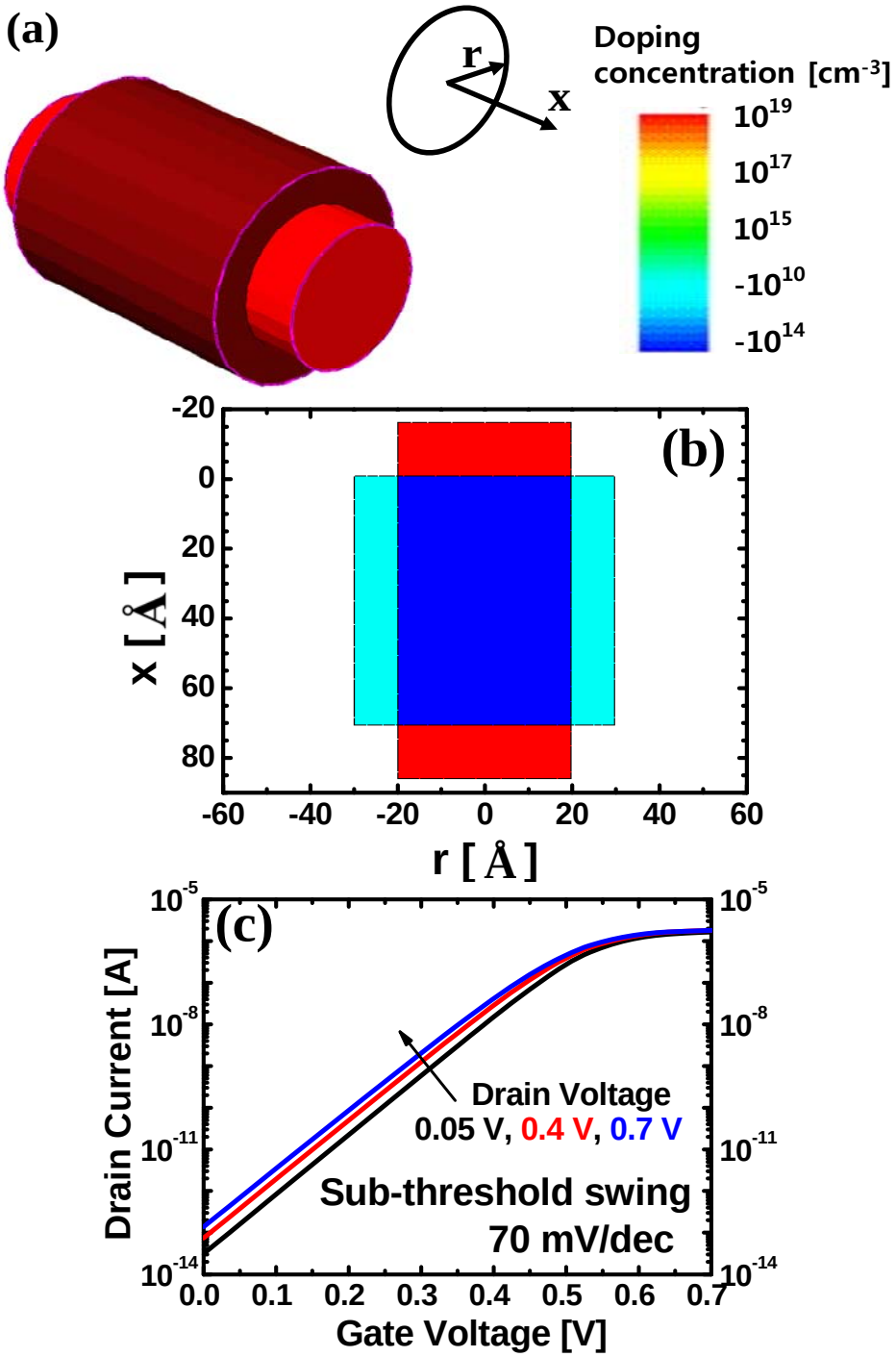


Fig. 2. 1. (a) Three-dimensional bird's-eye view of the nanowire FET (channel length = 70 Å, radius = 20 Å). (b) Cross-sectional view of the nanowire FET. (c) Input characteristic curves (I_D-V_G) for three different drain voltages (*i.e.*, 0.05 V, 0.4 V, and 0.7 V).

wire FET, a single trap is placed at (r_T, x_T),where r_T indicates the distance from the Si−SiO_2 interface to the trap, and x_T represents the distance from the source edge to the trap in the x−direction. Then, the drain current fluctuation in the nanowire FET is simulated for acceptor−like trap occupancy. The quantum confinement effect in the channel is taken into account using the van Dort quantization model. Also, the mobility values are concurrently adjusted with local doping concentrations, the degree of high field saturation, and the intensity of normal electric field.

2.2 Results

When a trap is filled with an electron captured from the channel, the threshold voltage in the 70-Å nanowire FET increases by ~50 mV (Fig. 2. 2a), so that there exists a non-negligible amount of drain current fluctuation (ΔI_D). Fig. 2b shows the conduction band diagram along the channel for the empty (black) and filled (red) trap conditions for the two different trap positions of x_T = 5 Å and 35 Å (r_T = 1 Å). The single electron captured at the trap significantly raises the conduction band energy level (see the two red-colored curves in Fig. 2. 2b) by ~0.2 eV. The impact of the single trap, filled with the captured electron, on the electron current density is clearly depicted in Fig. 2. 3 The two contour plots on the left-hand side in Fig. 2. 3 show the electron current density with the empty trap site in the r-x (upper) and r_y-r_z (lower) planes. On the right-hand side, the two contour plots show the electron current density with the filled trap site. When present, the single trap should significantly affect the drain current in the channel.

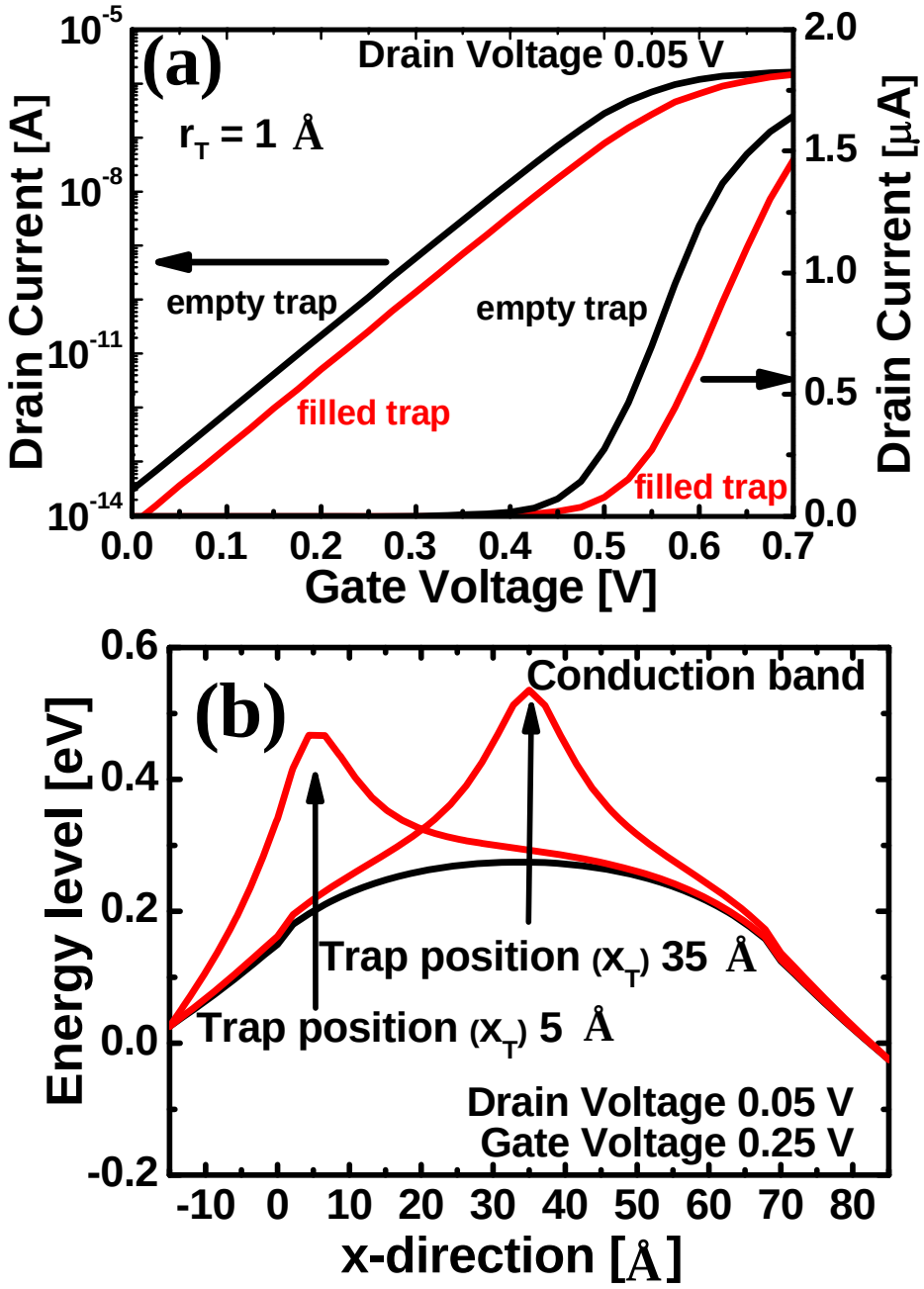


Fig. 2. 2. (a) I_D–V_G with an empty trap (black) and a filled trap (red). Note that the trap is located in the middle of the channel (*i.e.*, x_T = 35 Å) near the Si–SiO_2 interface (*i.e.*, r_T = 1 Å). (b) Conduction band shape along the channel for the empty (black) and filled (red) trap conditions for the two different trap positions of x_T = 5 Å and 35 Å. Note that r_T = 1 Å.

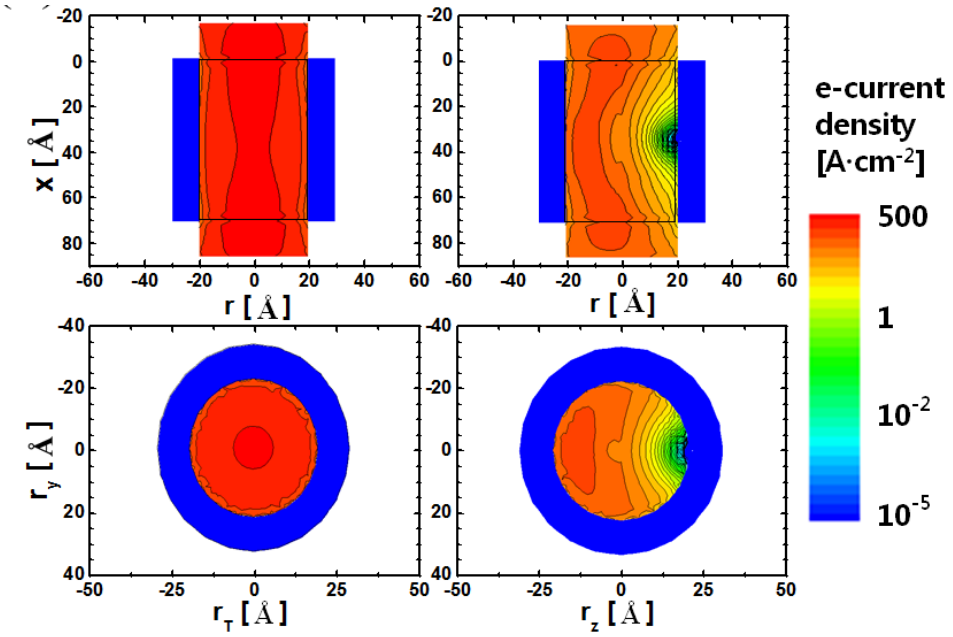


Fig. 2. 3. Contour plots for the electron current density along the channel when the trap at r_T = 1 Å, x_T = 35 Å is empty (see left−hand side) or filled (see right−hand side) at V_G = 0.25 V.

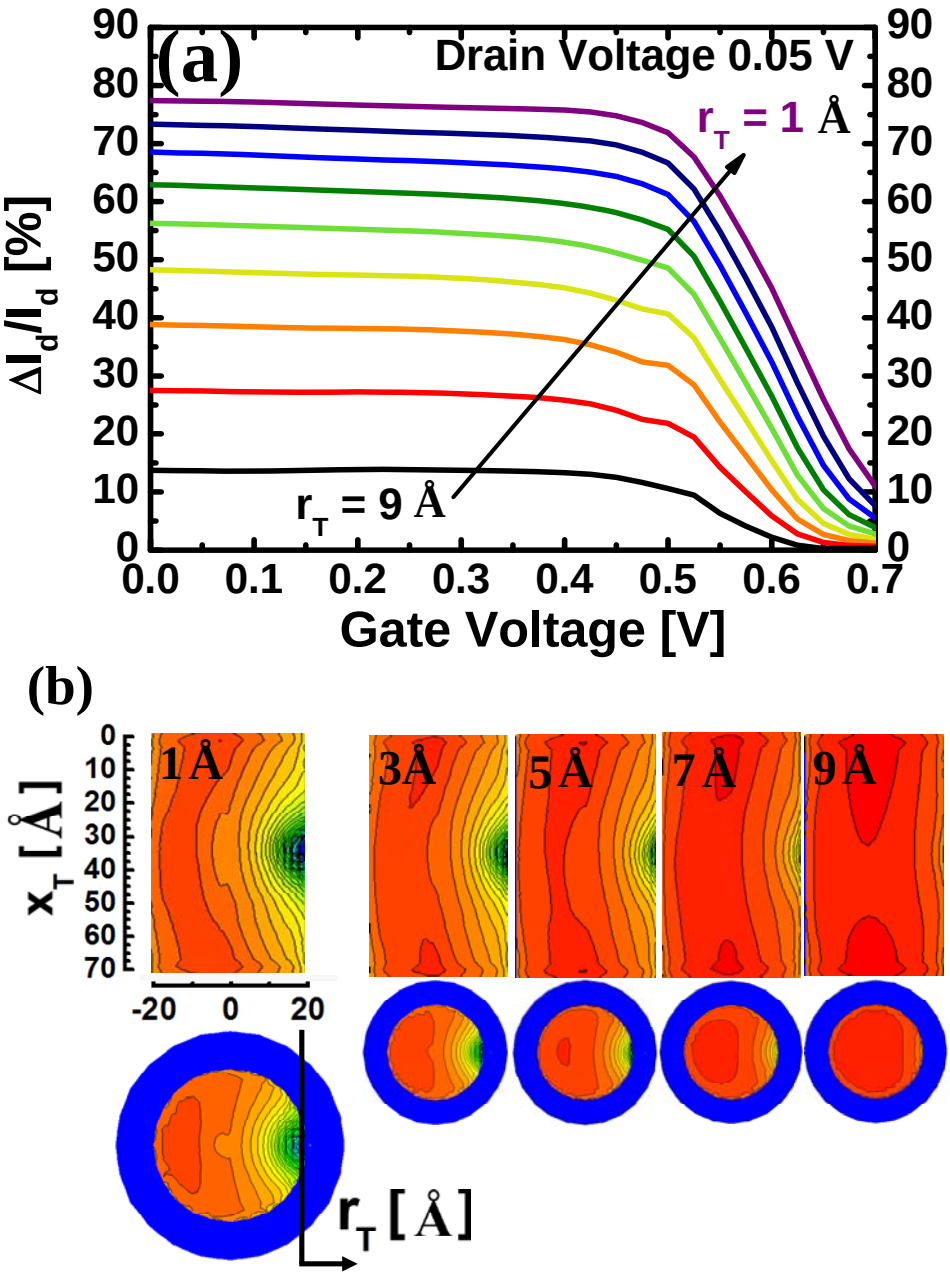
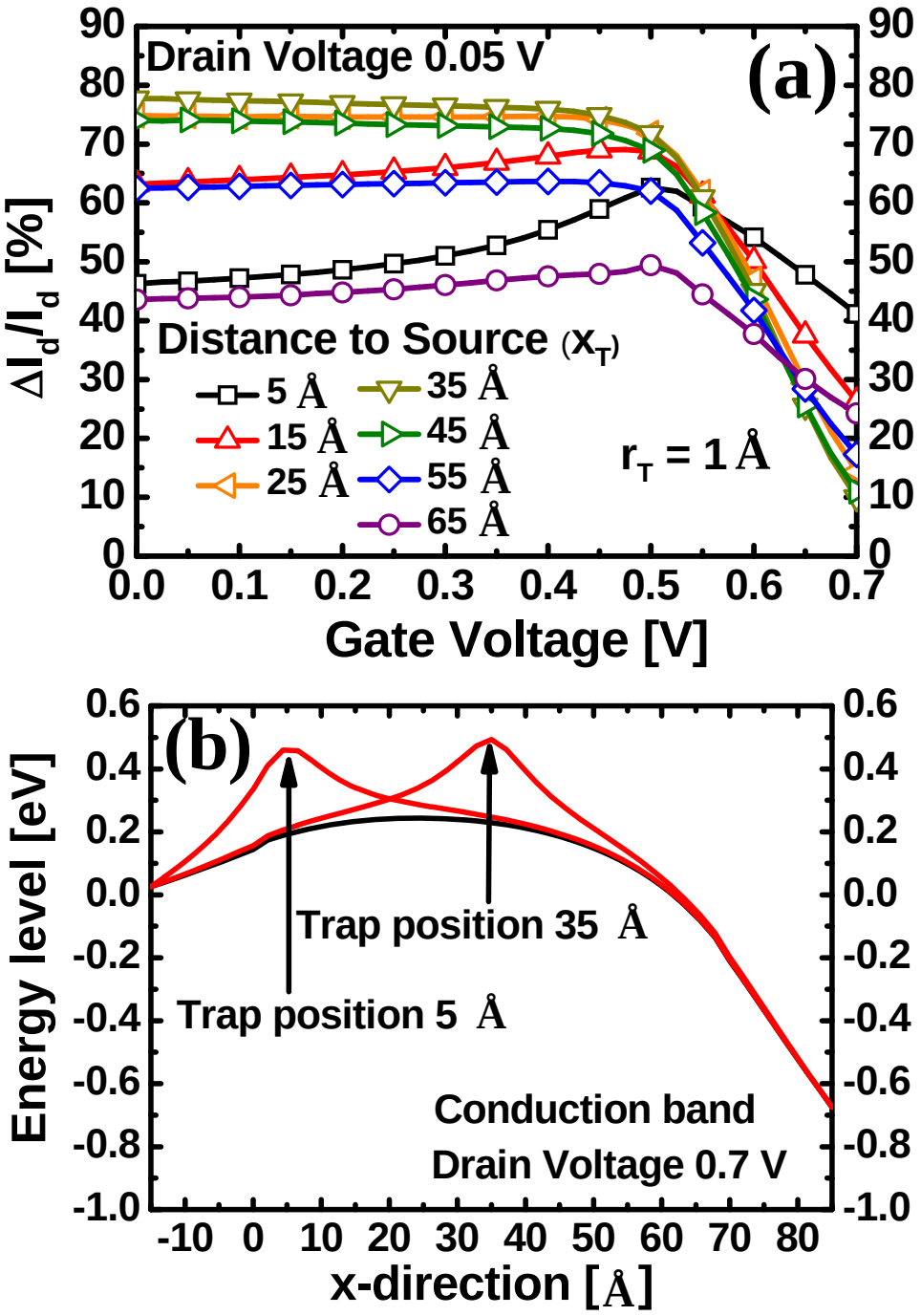


Fig. 2. 4. (a) $\Delta I_D/I_D$ *vs.* V_G with r_T = 1 Å to 9 Å in increments of 1 Å for x_T = 35 Å. (b) Contour plot for the current density with r_T = 1 Å to 9 Å in increments of 2 Å. Note that a lower current density flows near the trap (r_T, x_T) = (1 Å, 35 Å) because of increased distortion in the channel potential by the single filled trap resulting in a locally high threshold voltage.

Quantitatively, $\Delta I_D/I_D$ is ~78%, as shown in Fig. 2. 4a.

To investigate the effect of the trap position on the drain current, r_T is first varied from 1 Å to 9 Å for x_T = 35 Å. As shown in Fig. 2. 4a, the drain current varies between 13 % and 78% at V_G = 0.05 V. The performance variation in the 70-Å nanowire FET intensifies when the trap is close to the channel. The proximity of the trap to the Si-SiO_2 interface significantly distorts the channel potential, resulting in the local variation of the current density (Fig. 2. 4b). As is also shown in Fig. 2. 4a, the amplitude of RTN (*i.e.*, the drain current fluctuation) becomes large when the nanowire FET operates in the sub-threshold region [8]. This increase indicates that the channel potential is more sensitive to the trap because the gate-to-channel controllability is relatively smaller in the sub-threshold region.


Drain Voltage 0.05 V
(a)
Distance to Source (x_T)
5 Å
15 Å
25 Å
35 Å
45 Å
55 Å
65 Å
r_T = 1 Å
$\Delta I_d/I_d$ [%]
Gate Voltage [V]
(b)
Trap position 35 Å
Trap position 5 Å
Conduction band
Drain Voltage 0.7 V
Energy level [eV]
x-direction [Å]

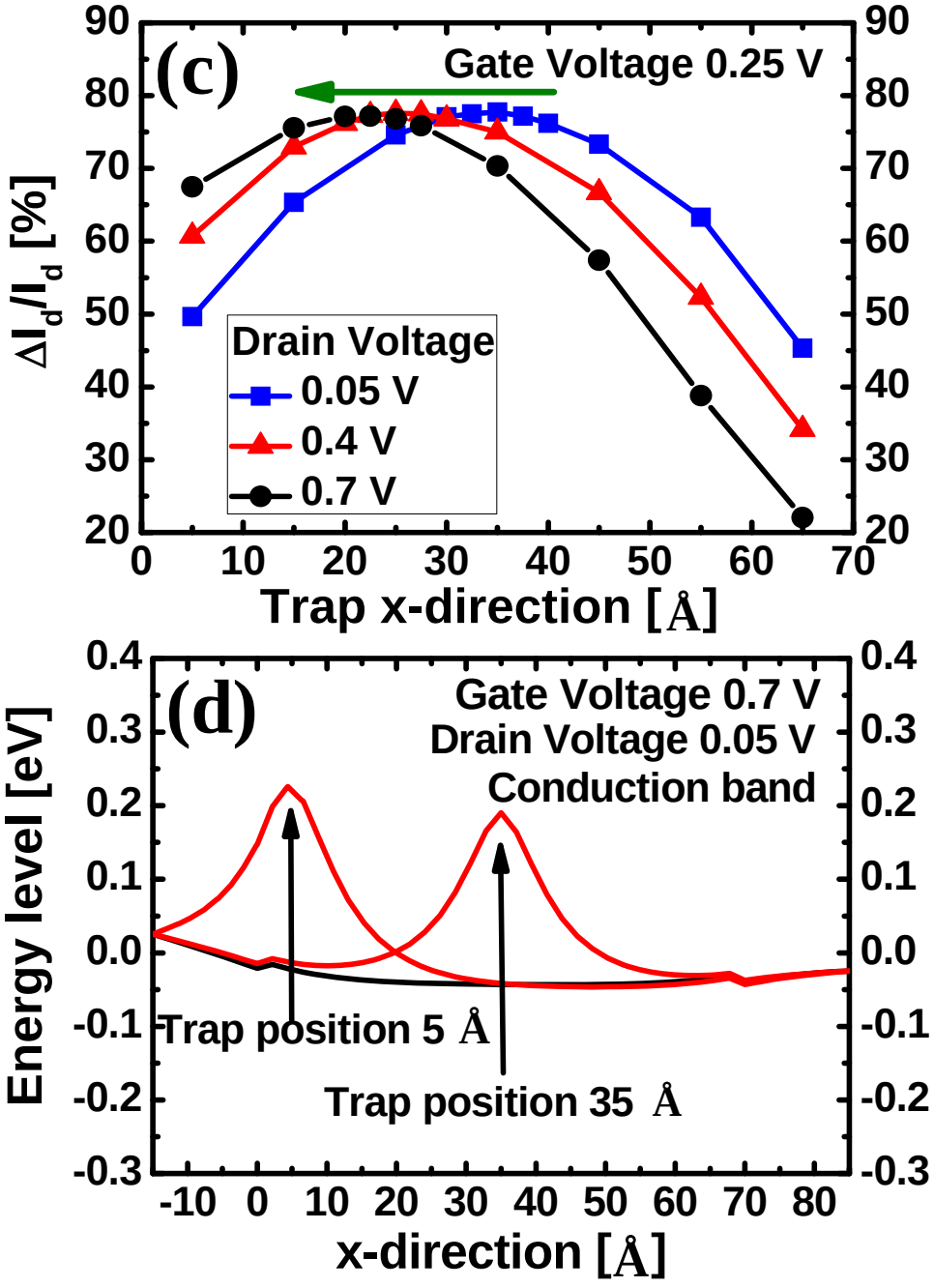


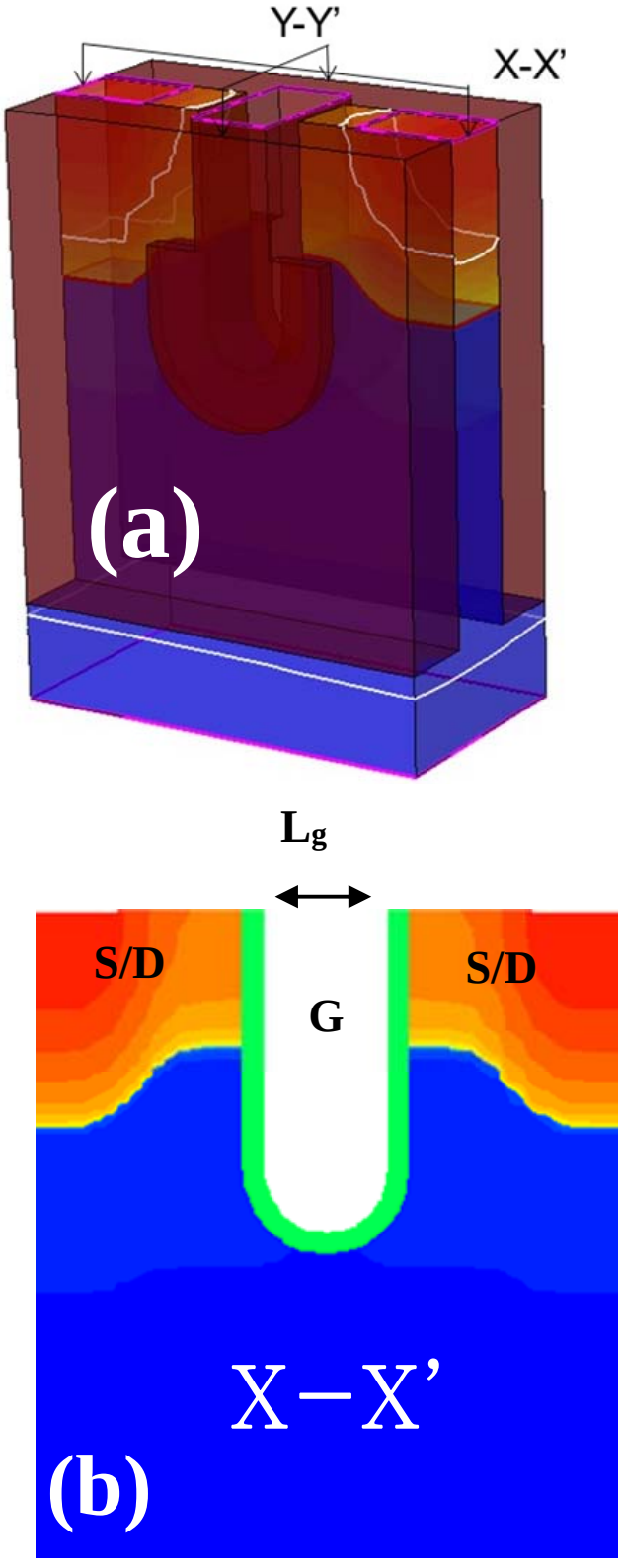
Fig. 2. 5. (a) $\Delta I_D/I_D$ *vs.* V_G with different values of x_T from 5 Å to 65 Å in increments of 10 Å. Note that r_T is 1 Å. (b) Conduction band diagram with an empty (black) or a filled (red) trap at V_D = 0.7 V and V_G = 0.25 V. Note that two trap positions are shown within the nanowire FET. (c) $\Delta I_D/I_D$ *vs.* x_T with various drain voltages (*i.e.,* 0.05 V, 0.4 V, and 0.7 V). (d) Conduction band diagram with an empty (black) and a filled (red) trap at V_D = 0.05 V and V_G = 0.7 V.

Fig. 2. 5a shows the effect of trap position along the channel (*i.e.*, in the x−direction from the source to the drain) on the drain current fluctuation at a drain voltage of 0.05 V with the trap located near the Si−SiO_2 interface at 1 Å (*i.e.*, r_T = 1 Å). Interestingly, $\Delta I_D/I_D$ for x_T = 5 Å and 65 Å (or 15 Å and 55 Å, or 25 Å and 45 Å) are almost same because of the symmetric conduction band in the channel (black−colored line in Fig. 2. 5b). However, as the drain voltage increases, the conduction band diagram becomes asymmetric (*i.e.*, the conduction band edge is lower on the drain side than on the source side), and therefore, the peak point for $\Delta I_D/I_D$ is shifted toward the source side (Fig. 2. 5c). Moreover, conduction band distortion due to the proximity of the trap to the source side (*vs.* the trap in the middle of the channel) occurs when the gate voltage increases from 0.25 V to 0.7 V (Fig. 2. 5b and 2. 5d). Hence, the impact of the trap position near the source and the Si−SiO_2 interface would be the most significant when the nanowire FET is operating in saturation mode.

3. Saddle device simulation

3.1 Saddle device design

Figure 3. 1(a) shows a 3-D schematic view of Saddle MOSFET. The overlapped side gate is defined near the source/drain (S/D) junction depth to reduce the GIDL current. Fig. 3. 1(b) and (c) shows the cross section views across the gate and the fin body, respectively. The LDD S/D junction depth is 21nm and the heavily doped S/D junction depth is about 33nm. The oxide thickness is 3.5nm. The fin body is directly connected to the substrate and the fin body thickness (W_{body}) is 20nm. The length of gate is fixed at 20nm. The uniform body doping is $1x10^{17}$ cm^{-3} and the LDD doping is $5x10^{18}$ cm^{-3}. The I-V curves show in figure 3. 2.


Y-Y'
X-X'
(a)
Lg
S/D
G
S/D
X−X'
(b)

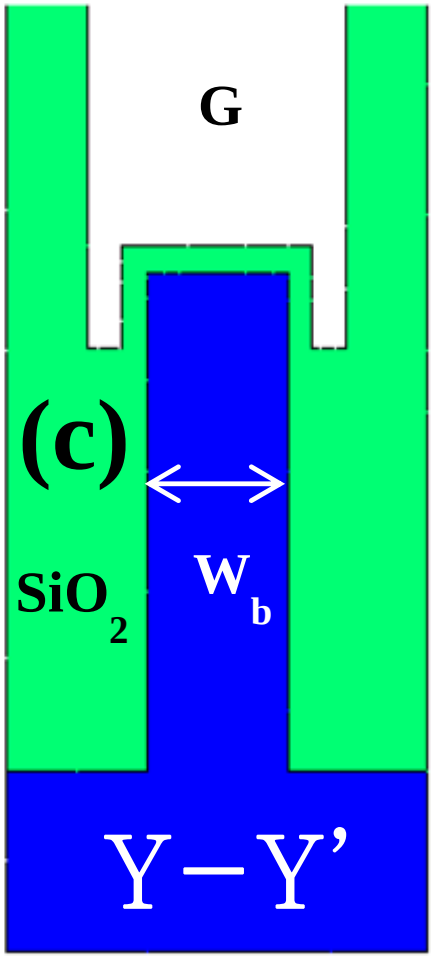


Fig. 3. 1. (a) 3-dimensional structure of Saddle MOSFET (b) Cross section view across the gate (X-X') (c) Cross section view across the fin body (Y-Y')

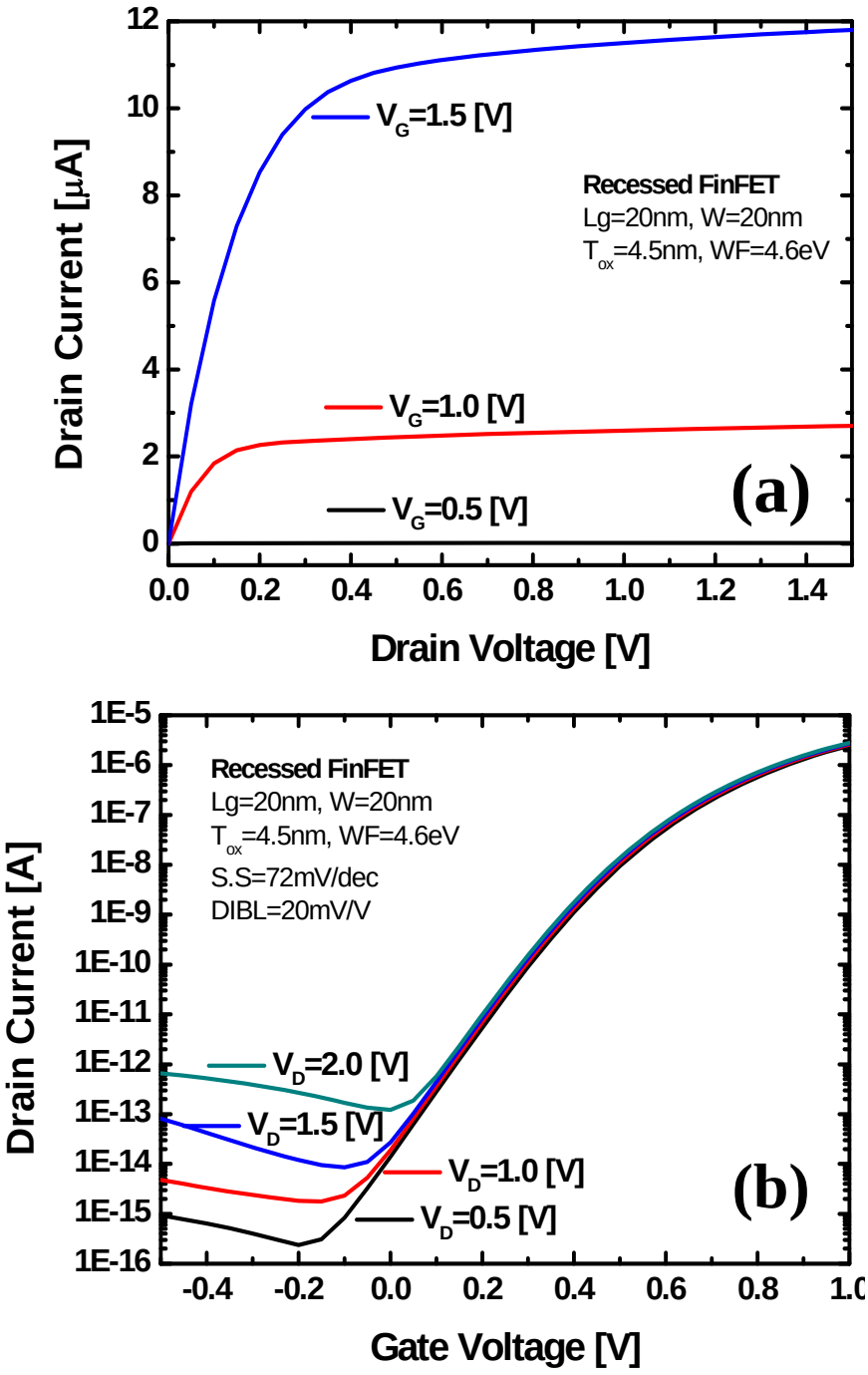


Fig. 3. 2. I-V curves of structure of Saddle MOSFET (a) I_D-V_D curve (b) I_D-V_G curve

3-Dimensional simulation is performed by using TCAD. We use doping dependence mobility model and velocity saturation mobility model for I-V simulation. Also, we choose the hurkx model about band to band tunneling and trap assisted tunneling model in gate-induced drain leakage current simulation.

3.2 Results

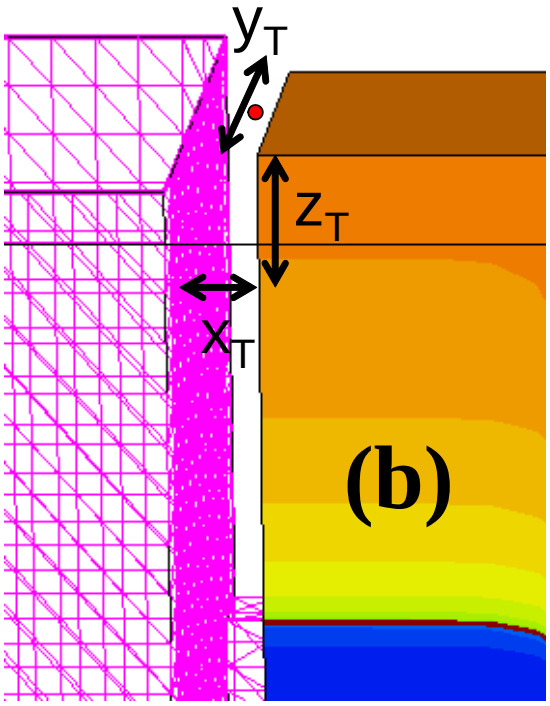
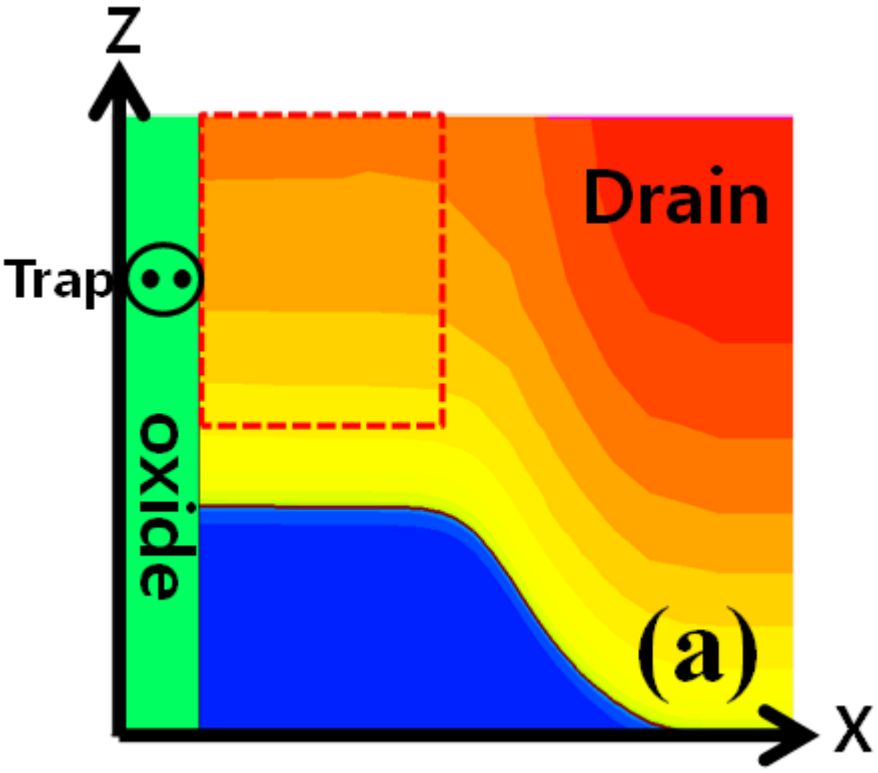


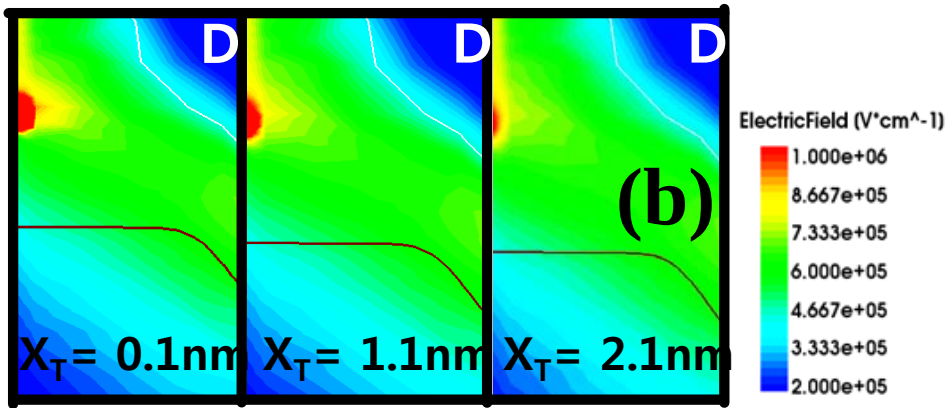
Fig. 3. 2. Location of a simulated oxide trap at gate-to drain overlap region

A simulated oxide trap is located inside the gate oxide on the gate to drain overlapped region as shown in Fig. 3. 2 At every trap's position, we investigate the difference between GIDL current when the trap is neutral and charged with an electron having charge of $-1.602\text{x}10^{-19}$C.

Figure 3. 3(a) is the cross section view across the fin

middle(Y=10nm). If an electron is captured by an oxide trap in the gate-to-drain overlaped region, the electric field at the Si/SiO_2 interface increases as shown in Fig.3. 3(b). The increased electric field leads to the tunneling more easily so the GIDL current increases. In Fig. 3. 3(c), when the trap is located at x_T=0.1nm, the amplitude of ΔI/I is about 32% while the trap is at x_T=2.1nm, the amplitude of ΔI/I is about 1%. The amplitude of ΔI/I with x_T=2.1nm trap is very small due to the energy level of conduction band with trap does not change compared with the conduction band without trap as shown in Fig. 3. 3(b). To estimate the highest amplitude of ΔI/I, we locate the trap at x_T=0.1nm and we continue to investigate the trap' s position by width direction from y_T=0~20nm.


Z
Drain
Trap
oxide
(a)
X


D
D
D
(b)
X_T= 0.1nm
X_T= 1.1nm
X_T= 2.1nm
ElectricField (V*cm^-1)
1.000e+06
8.667e+05
7.333e+05
6.000e+05
4.667e+05
3.333e+05
2.000e+05

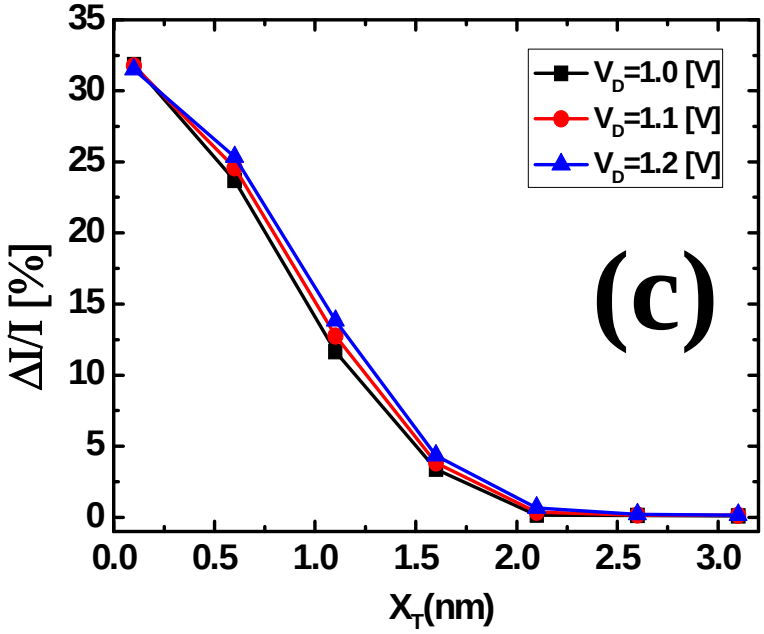
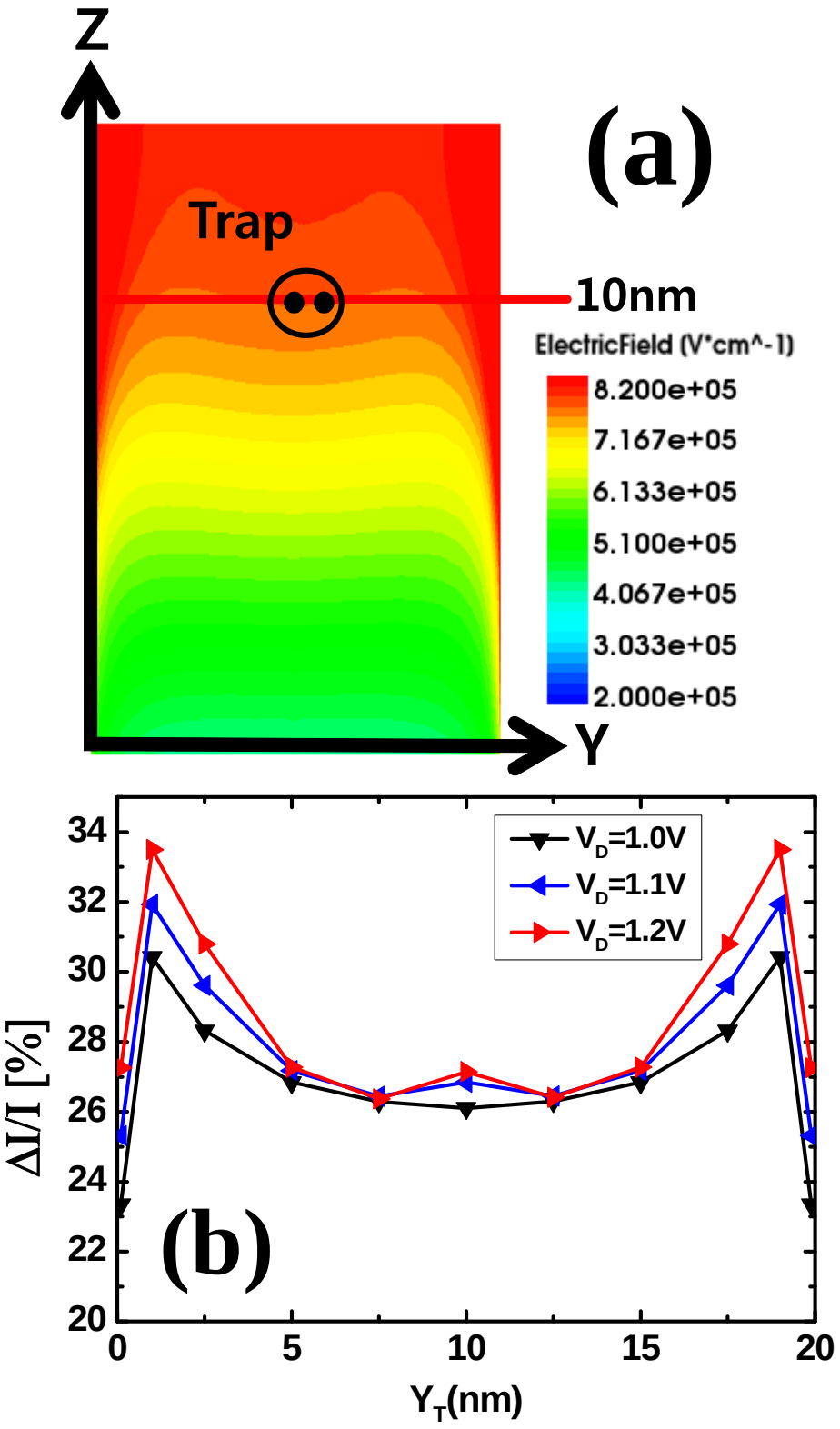


Fig. 3. 3. (a) cross section view across the fin middle(Y=10nm) (b) ΔI/I dependence on the trap location by lateral direction: x_T (c) The energy level of conduction band increases significantly at the interface when the oxide trap is at 0.1nm and it does not change when the trap is at 3nm.


Z
(a)
Trap
10nm
ElectricField (V*cm^-1)
8.200e+05
7.167e+05
6.133e+05
5.100e+05
4.067e+05
3.033e+05
2.000e+05
Y
34
32
30
28
26
24
22
20
ΔI/I [%]
V_D=1.0V
V_D=1.1V
V_D=1.2V
(b)
0
5
10
15
20
Y_T(nm)

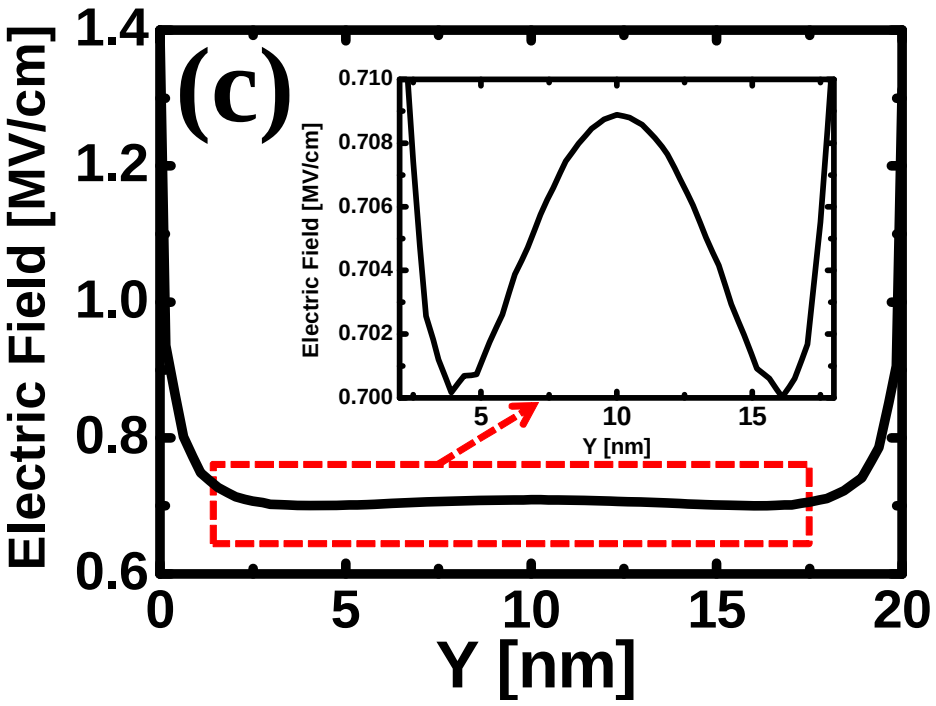


Fig. 3. 4. (a) Cross section view of electric field across the Si/SiO_2 interface (Y−Z plot) (b) ΔI/I dependence on the trap location by width direction– y_T (c) Electric field on the width direction (Z=10 nm)

The amplitudes of ΔI/I at the edges of fin body are higher than the other positions inside the body. At V_{DG}=1.2 V, the highest amplitude of ΔI/I is about 34% at x_T=0.1nm, y_T = 1nm. The distribution of ΔI/I values are quite symmetric by width direction as shown in Fig.3. 4(b). The highest points of ΔI/I is located same with the highest points of electron current density, near the corner of fin body as shown in Fig.3. 4(a).

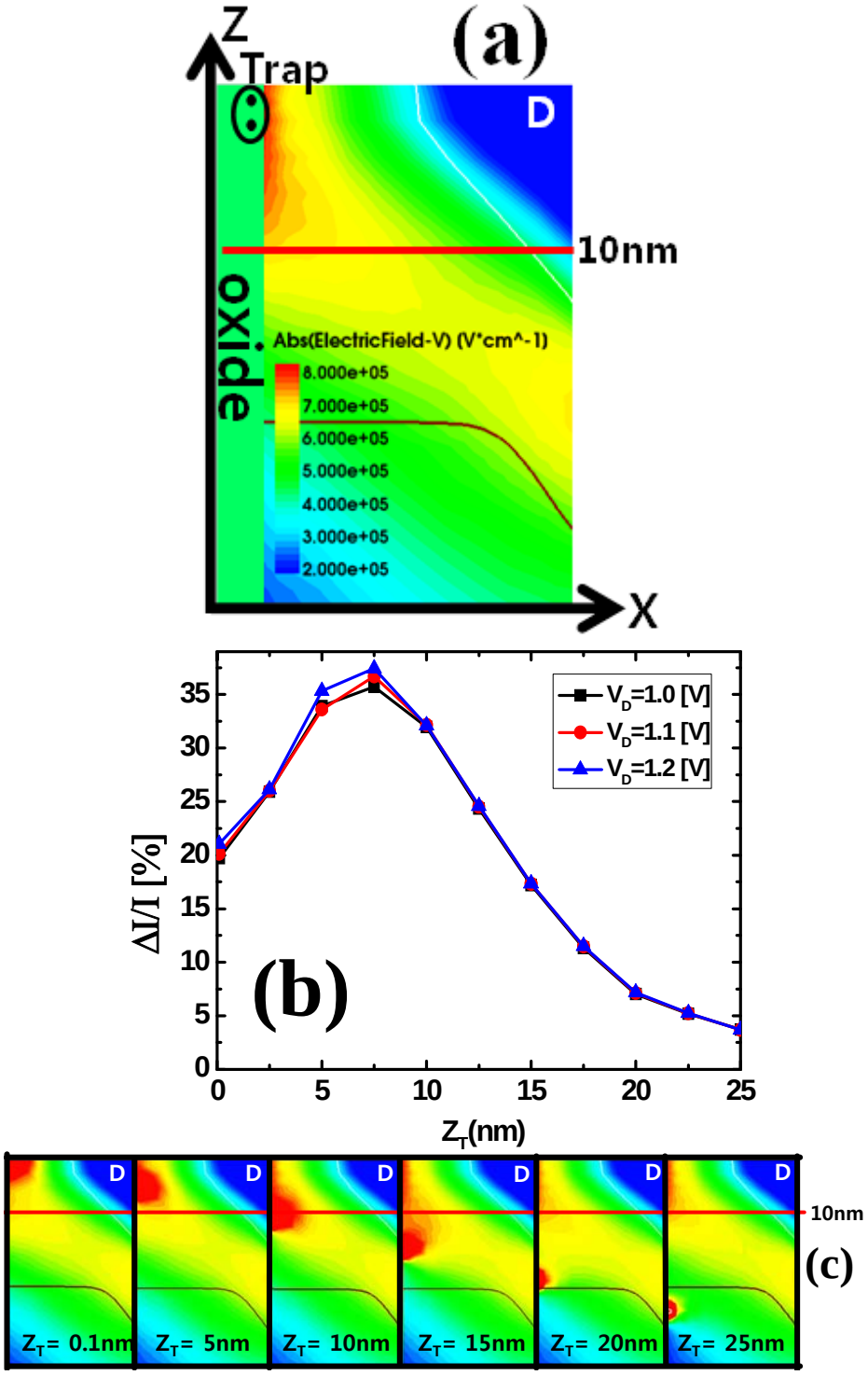


Fig. 3. 5 (a) cross section view across the fin middle(Y=10nm) (b) ΔI/I dependence on trap location by vertical direction – z_T (c) The contour of electron current density by vertical direction

We continue investigating the ΔI/I from z_T=0~20nm by vertical position with a trap fixed at x_T=0.1nm and y_T=1nm. As shown in Fig.3. 5(b), the highest amplitudes is 38% at z_T=5nm and the distribution of ΔI/I is same with the contour of electron current density by vertical direction in Fig. 3. 5(c).

Previous paper focused on the RTN effect depending the trap position of MOSFET device through simulation [22]. In this paper, we studied the RTN effect depending the trap position of nano-wire and Saddle device. In MOSFET case, ΔI/I amplitude is about 5%. In nano-wire and Saddle device case, ΔI/I amplitude is respectively 78%, 36%.

4. Conclusion

Previous paper focused on the RTN effect depending the trap position of MOSFET device through simulation. In this paper, we studied the RTN effect depending the trap position of nano-wire and Saddle device. In MOSFET case, ΔI/I amplitude is about 5%. In nano-wire and Saddle device case, ΔI/I amplitude is respectively 78%, 36%. The small size novel devices should be considered the RTN effect. In device operation case, we can calculate the amplitude of ΔI/I and anticipate the location of trap using this paper result.

The effect of a single trap on the device performance in a 70-Å silicon nanowire FET has been investigated using 3-D TCAD simulations. The impact of the position of the trap on the drain current fluctuation has been quantitatively analyzed. The highest drain current variation (*i.e.*, $\Delta I_D/I_D$ ~ 78%) was observed when the trap was placed near the source side and close to Si-SiO_2 interface.

Finally, the peak point for the $\Delta I_D/I_D$ was shown to shift from the middle of the channel toward the source side with an increase in the drain voltage. In nanowire device, the device radius size is smaller than previous size for increasing gate controllability. But, we studied the trade-off characteristics between the device size and the RTN effect. Hence, the device radius size couldn't smaller if you didn't consider the RTN effect.

We investigated the RTN in GIDL current of Saddle MOSFET, a promising candidate for highly-density DRAM application. We found that the highest value of $\Delta I/I$ is about 36% with a single electron captured at V_{DG}=1.2V. In Saddle device, we find the trap position of maximum $\Delta I/I$. Therefore, modified process in that position will make better performance in device.

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초 록

70-Å 나노와이어 field-effect transistor (FET)를 10나노 이하 CMOS 기술을 바탕으로 디자인하였고 그 소자에서 단일 산화막 트랩에 의한 random telegraph noise (RTN) 영향을 시뮬레이션을 통해 연구하였다. 단일 전자에 의한 드레인 전류의 변화폭($\Delta I_D/I_D$)은 나노와이어 소자에서 최대 78 %까지 증가함을 보았다. 또한, 여러 산화막 트랩의 위치에 따라 RTN현상이 나노와이어 소자에서 어떻게 달라지는지를 연구하였다. 여러 드레인, 게이트 전압조건에 따라서 분석을 진행하였다. 만약 드레인 전압이 증가하면 $\Delta I_D/I_D$ 의 최대값 지점은 소스쪽으로 이동하게 된다. 이 영향을 설명하기 위해 여러 위치조건에서 트랩에 전자 한 개가 차게되면 전자의 농도 분포와 전도대 밴드 에너지의 상태를 연구했다..

DRAM 소자로 각광받고 있는 Saddle MOSFET을 디자인 하였고 Gate Induced Drain Leakage (GIDL) RTN현상을 삼차원 시뮬레이션을

통해 관찰하였다. 여러 산화막 트랩의 위치에 따라 RTN현상이 Saddle 소자에서 어떻게 달라지는지를 연구하였다. 이 영향을 설명하기 위해 여러 위치조건에서 트랩에 전자 한 개가 차게 될 때의 전계 분포를 연구했다.

주요어 : 나노와이어, Saddle, Random Telegraph Noise (RTN), 삼차원 컴퓨터 시뮬레이션, 트랩.

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